



Docket No.: 95-528

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

SHEN *et al.*

Serial No.: 10/790,205

Filed: March 2, 2004

Group Art Unit: (Not Assigned)

Examiner: (Not Assigned)

For: FAST FOURIER TRANSFORM CIRCUIT HAVING PARTITIONED MEMORY FOR  
MINIMAL LATENCY DURING IN-PLACE COMPUTATION

**LETTER SUBMITTING FORMAL DRAWINGS**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

The undersigned hereby submits the attached five (5) sheets of formal drawings.

Respectfully submitted,

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**Date: April 21, 2004**